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(54) Digital beam-forming radar

(57) A digital beam-forming radar including an array (10) of receiver antenna elements, each element feeding a zero i.f. channel (11) in which signals received from the element are sampled at a sub-pulse rate and digitised into one-bit words. Groups on one-bit words are then presented as multi-bit addresses to memories (12) in a first beam-forming stage. The memories hold look-up tables to which weighting functions have been applied by a beam controller (13). The memory outputs are in the form of code words which are then integrated in accumulators 14 to provide code words at the pulse rate. Secondary groups of code words can be similarly used as addresses in a second beam forming stage (15), subsequent third stage beam forming (16) being accomplished in a main processor (17) where pulse compression, Doppler filtering and detection functions are implemented.

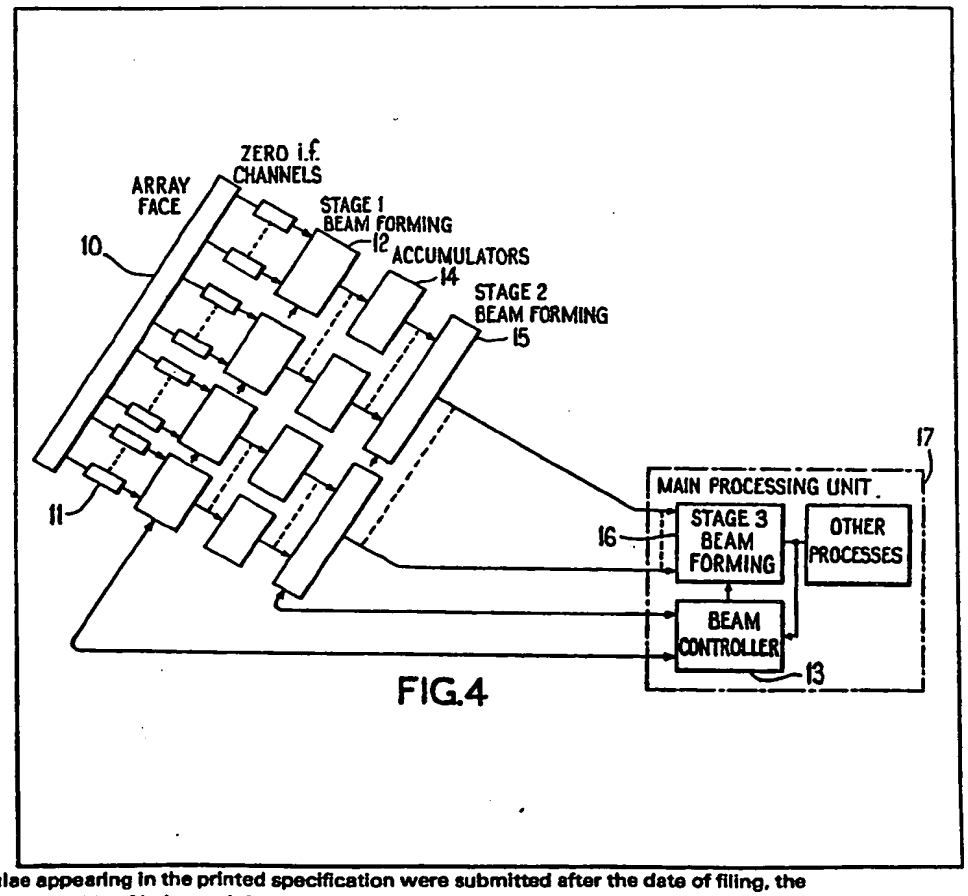

FIG.4

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Certain of the mathematical formulae appearing in the printed specification were submitted after the date of filing, the formulae originally submitted being incapable of being satisfactorily reproduced.
The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.
This print takes account of replacement documents later filed to enable the application to comply with the formal requirements

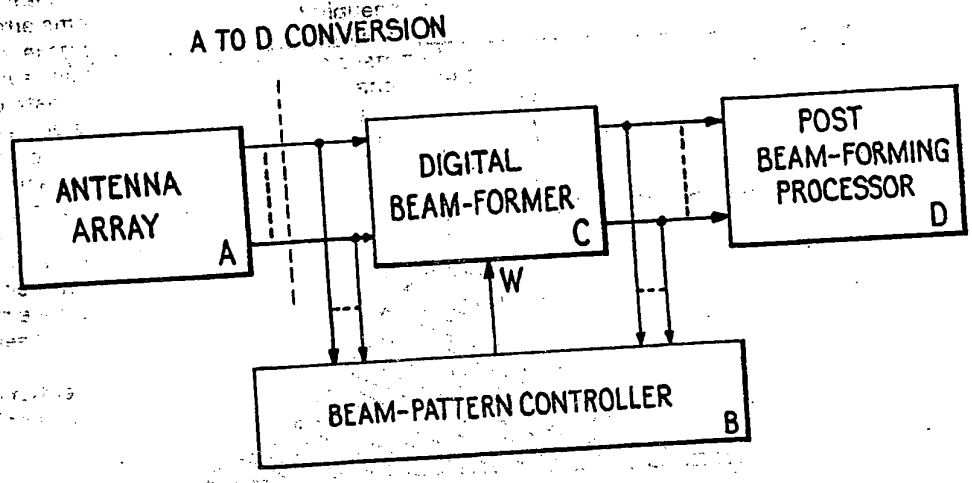

FIG.1

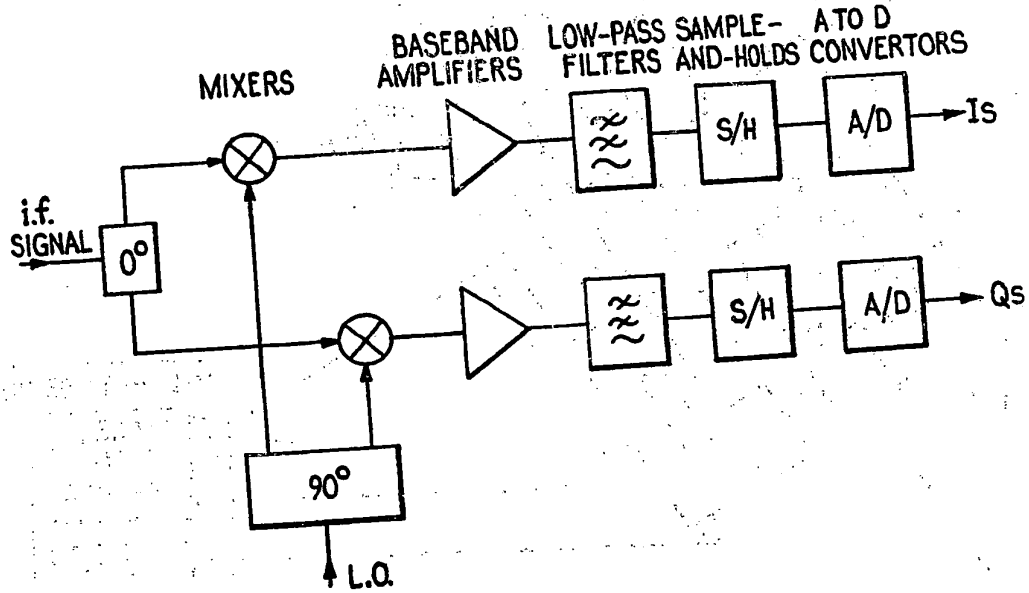

FIG.2

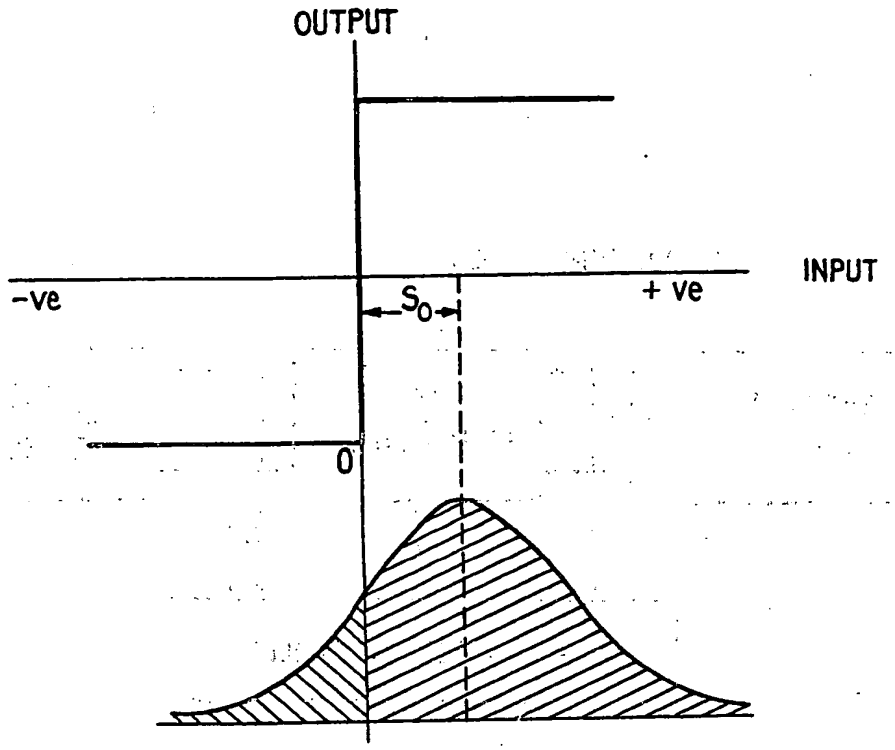

FIG.3

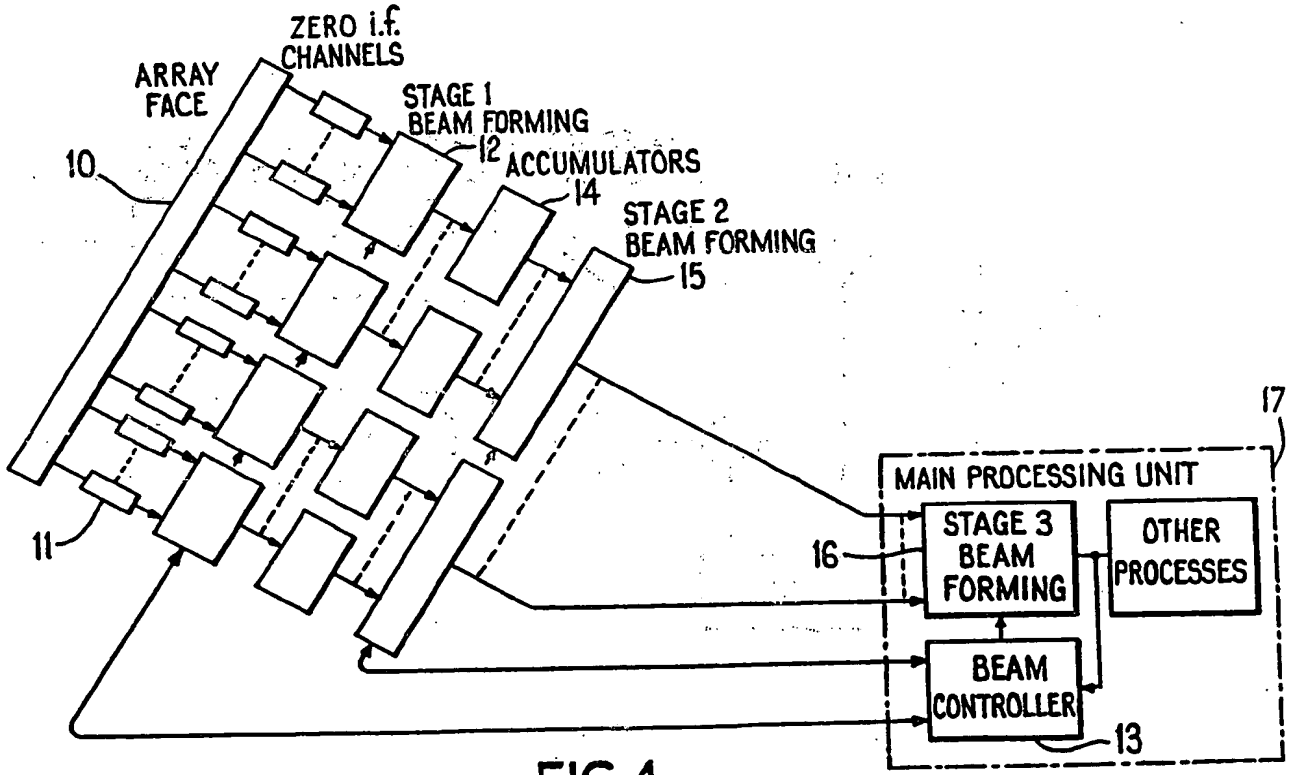

FIG.4

SPECIFICATION

Digital beam-forming radar

This invention relates to a digital beam-forming radar of the type in which the outputs from an array of receiver antenna elements are weighted and combined in a predetermined manner so that the array provides the desired beam forming function.

The use of digital techniques in the control and formation of spatial beams in an array radar can be of benefit to both the transmit and receive functions. In general, however, considerably more processing power is available in the employment of such techniques to a receive-array radar. The advantages and flexibilities include, for example, the availability of simultaneous search and track functions, multiple beam outputs, adaptive null steering against multiple jammers, ultra-low sidelobe performance, and the possibility of beam-pattern variation as a function of range. For a large array, calibration of channels to compensate for phase and amplitude drifts can also be performed more readily by digital techniques.

According to the present invention there is provided a digital beam-forming radar including an array of receiver antenna elements, means for simultaneously sampling the signals received at all the elements, individual digitising means for each element whereby successive signal samples received from each element are converted into respective one-bit digital words, a first beam-forming stage wherein first groups of simultaneously occurring digital words are presented in the form of multi-bit addresses to memories individual to each group, each memory holding predetermined look-up tables whereby each group address causes a first unique corresponding digital code word to be output from the memory, and means for applying the outputs of the first beam-forming stage to further beam forming stage(s).

The invention further provides a method of digital beam-forming in a radar having an array of receiver antenna elements including the steps of simultaneously sampling the signals received at each of the elements, individually digitising the sampled signals into respective one-bit digital words, applying first groups of simultaneously occurring digital words to memories individual to each group whereby each group forms a multi-bit address for a memory, each memory holding predetermined look-up tables whereby each address causes a unique corresponding digital code word to be output from the memory.

The invention will be described with reference to the accompanying drawings, in which:—

Fig. 1 illustrates in generalised block form a fully digital receive-array radar having a beam forming function,

Fig. 2 illustrates the usual circuit configuration for the digitisation of the output from one antenna element,

Fig. 3 illustrates the principle of 1-bit digitisation of a single channel, and

Fig. 4 illustrates a system schematic for a fully receive array according to the invention.

The generalised system shown in Fig. 1 consists functionally of four main blocks:

(i) an antenna array of receive modules A,

(ii) a beam-pattern controller B,

(iii) a digital beam former C, and

(iv) a post beam-forming processor D.

The beam-pattern controller, usually in the form of a general or special purpose digital processor, takes in digital words from either A or C, or both, as input information, and from it generates output weight values which determine the beam shape in C. Control can either be of the open-loop type, if the input is derived purely from A; or of closed-loop type if the controller has access to the output of the beam former C. A number of adaptive techniques could be used in this case to optimise the system performance according to changes in the receive environment, see for example "Adaptive Array Principles", Hudson J. E., IEE Electromagnetic Wave Series, Peter Peregrinus Ltd., 1981.

Although the output from A to C has to be at least at the Nyquist sampling rate appropriate to the signal bandwidth to preserve the information, sampling for the beam-pattern controller can be done at a significantly lower rate, since the radar environment is unlikely to change at a rate comparable to the signal bandwidth. In this way, a processor of moderate power may be sufficient for discharging the controller function, in contrast to the requirement of the beam former itself.

Digitisation of the receive element outputs is conveniently done at baseband using the zero i.f. technique, as shown in Figure 2. The incoming signal at an intermediate frequency (i.f.) is split into two paths, called the in-phase (I) and Quadrature (Q) paths, and mixed with two local oscillator (L.O.) inputs in quadrature, at the i.f. frequency. The resultant baseband signals are amplified separately, filtered to the appropriate bandwidth, sampled and held, and then turned into the in-phase and quadrature output words, Is and Qs, by two analogue to digital (A/D) convertors.

For an array of, say, a few thousand elements, the number of zero i.f. channels and associated A/D convertors required will be substantial. One way of reducing circuit complexity is to employ partial analogue beam-forming prior to digitisation. A certain amount of beam control is also possible by the beam controller. The present invention, however, is entirely concerned with the wholly digital solution.

The digital beam former C takes in the signal vectors (Is, Qs) from A, and combines them with the weight vectors (Iw, Qw) from B, to form the output vector Io, Qo), according to the expressions:

$$I_o = \sum_{1}^{n} I_s I_w - Q_s Q_w \quad (1)$$

$$Q_o = \sum_{1}^{n} I_s Q_w + Q_s I_w \quad (2)$$

where n is the number of element inputs used in the process. n is not necessarily the same as the total number of elements N, as the beamforming is usually done is successive stages for large values of N.

One way of implementing the beam former structure is by a Discrete Fourier Transform (DFT) or a Fast Fourier Transform (FFT) as disclosed in "Theory and Application of Digital Signal Processing", Rabiner L.R. and Gold B., Prentice Hall, 1975. The main components required are fast digital multiplier-accumulators. Although the FFT is more efficient in hardware terms, this may not necessarily be the best choice, as the number of output beams required is usually fewer than the number of inputs. The DFT, or some other look-up table method, may be found to be more appropriate, as will be shown below.

The post beam-forming processor D includes the pulse compression, Doppler filtering, and detection functions. Pulse compression can be performed by digital correlators, and Doppler filtering by an FFT processor. As the beam-forming process reduces significantly the number of signal paths, saving in hardware is achieved by performing these two functions after beam-forming. This, however, requires that the beam-forming be executed at the uncompressed data rate, placing a very heavy loading on its hardware.

Coherent integration in the receiver system is provided for by the three operations: beam-forming, pulse compression, and Doppler filtering. If the total number of elements is N, number of chips in the compression code is C, and the number of Doppler cells is D, the processing gain of coherent signals relative to random noise after the above operations is:

$$G = 10 \log_{10} (NCD) \text{ dB} \quad (3)$$

If the input word-length after digitisation is L_1, the integration process also increases the resolution of the system to an output word length L_2, such that

$$L_2 = L_1 + \tfrac{1}{2} \log_2 (NCD) \quad (4)$$

Consider an example of a representative surveillance radar with a rectangular array of 64 by 64 elements, using a 32 bit compression code of 10*S per bit, and with 32 Doppler output cells. The processing gain is, by (3), 66 dB.

Supposing a minimum signal to noise ratio (SNR) of 13 dB is required for positive detection after processing, the weakest detectable signal is some 53 dB below the noise floor at the digitisation point. Even a signal 40 dB above the minimum is still 13 dB below noise. This leads one to question whether proper A/D convertors are really necessary for the digitisation process. It may well be that a 1-bit digitiser, in the form of a zero-crossing detector, is sufficient, in which case an enormous saving in hardware cost is possible. A 1-bit digitiser produces a logical '1' when the input is positive and a '0' when the input is negative, or vice versa.

An added bonus of this scheme is that the dynamic range of the i.f. channels preceeding need only be very small, in fact just large enough to allow the zero-crossing mechanism to be operational.

Figure 3 shows how a 1-bit channel can be used to give an adequate representation of a signal voltage S_o. With Gaussian noise of standard deviation σ superimposed on the signal, the output can be represented by the difference in the two shaded areas separated by the zero line, if a sufficiently large number of samples are accumulated to allow the effect of the probability distribution to be felt.

With a distribution of noise

$$Z(x) = \frac{1}{\sqrt{2\pi\sigma}} \exp\left(-\frac{x^2}{2\sigma^2}\right) \quad (5)$$

the probability of having a negative output is given by

$$P_1(x) = \frac{1}{\sqrt{2\pi}\sigma} \int_{-\infty}^{S_o} \exp\left(-\frac{x_2^2}{2\sigma^2}\right) dx \quad (6)$$

$$= \tfrac{1}{2}\left\{1 - \mathrm{erf}\left(\frac{S_o}{\sqrt{2}\sigma}\right)\right\}$$

Similarly, the probability of a positive output is given by

$$P_2(x) = \tfrac{1}{2}\left\{1 + \mathrm{erf}\left(\frac{S_o}{\sqrt{2}\sigma}\right)\right\} \quad (7)$$

If the positive and negative outputs are represented by +1 and −1 volts respectively, the mean signal at the output is given by

$$\langle y_o \rangle = \mathrm{erf}\left(\frac{S_o}{\sqrt{2}\sigma}\right) \quad (8)$$

$$= \frac{2}{\sqrt{\pi}}\left\{\frac{S_o}{\sqrt{2}\sigma} - \frac{1}{3}\left(\frac{S_o}{\sqrt{2}\sigma}\right)^3 + \frac{1}{5.2}\left(\frac{S_o}{\sqrt{2}\sigma}\right)^5 - \right\} \quad (9)$$

For $S_o << \sigma$, this transfer curve approaches a straight line, and provided input signals are operated within this region, good linearity is maintained.

Poor linearity, on the other hand, leads to the generation of intermodulation products between input signals. Supposing there are two signals, S_1 and S_2, with with $S_1 > S_2$, it can be shown that, as a guidance, a minimum of about −9 dB of SNR is required for S_1 at the input in order to give an output intermodulation of −30 dB relative to S_2, the weaker signal. The system, therefore, requires that the maximum signal level before digitisation be at a minimum of 9 dB below the noise floor.

The hard-limiting will also lead to a degradation in output SNR. This is given by

$$SN_o = \frac{\langle Y_o \rangle^2}{\langle Y_o^2 \rangle - \langle Y_o \rangle^2}$$

$$= \frac{\mathrm{erf}^2\left(\frac{S_o}{\sqrt{2\sigma}}\right)}{1 - \mathrm{erf}^2\left(\frac{S_o}{\sqrt{2\sigma}}\right)}$$

The input SNR is

$$SN_i = \frac{S_o^2}{\sigma 2}$$

$$\text{Hence } SN_o = \frac{\mathrm{erf}^2\left(\frac{\sqrt{SNi}}{\sqrt{2}}\right)}{1 - \mathrm{erf}^2\left(\frac{\sqrt{SNi}}{\sqrt{2}}\right)}$$

If the linearity criterion above has already been satisfied, then, from (9)

$$SN_o \approx \frac{2}{\pi} SN_i$$

leading to a degradation of approximately 2 dB. The use of 1-bit digitisation to detect signals lying below the noise floor is disclosed in our prior patent application 8134090 (A.C.C. Wong-6).

If 1-bit digitisation of the received signal is used, an elegant way of implementing the first stage of the digital beamformer via look-up tables will follow naturally. Returning to our example system, suppose each group of 4 by 4 elements is combined to form one intermediate output, then there would be 2^{16} possible input combinations. These can be used to address a block of memory, where all the pre-calculated possible output combinations are stored. From (4), the output needs be of 3-bit precision. The memory size required is therefore 64k x 3 bits for each of the I and Q channels, most conveniently accommodated by three 64K random access memory chips. The throughput time of the block is the access time of the memory.

By using two sets of random-access memory (RAM) chips in a switched arrangement, instantaneous change in beam shape can be realised.

The 4 x 4 group need not consist of adjacent elements only. Because of the complete freedom is assigning the contents of the RAMs, the elements of each group can be taken from anywhere within the array face, and would lead to greater system flexibility, especially if the elements are located on a non-uniform grid.

The next stage of beam-forming may be used to combine the outputs of the sixteen stage-1 blocks in a horizontal row into one block to complete the beam-forming in the azimuth plane. 16 stage-2 blocks are thus arrived at. This is formed by a third stage completing the beam-forming in the elevation plane.

Both stage 2 and stage 3 blocks can be realised by additional look-up tables. The input words are now no longer signal-bit, leading to a much longer address length, and therefore prohibitively large memory size, if direct look-up is required. This can be overcome by the linear binary decomposition principle which is explained below.

Since beam-forming is a linear process, we can slice the collection of multi-bit input words into groups of single bit significance, apply each group in turn to the memory address, and recombine the subsequent outputs from all the look-up operations with the appropriate weightings to arrive at a resultant output. Since the significance of the successive bits are in powers of 2, recombination with the proper weighting is a simple operation. Such a technique is disclosed in our prior patent application 8134091 (A.C.C. Wong-7).

The throughput rate, compared with a direct look-up, is reduced by a factor equal to input word-length. This, however, is done at an exponential reduction in memory size, and is therefore worthwhile in hardware terms. The power dissipation of this scheme is usually less than a conventional FFT solution of an equivalent throughput.

The fact that the signal level needs to be kept below the noise floor at the digitisation point places an upper bound on the maximum signal that the system can handle satisfactorily. With jammer and clutter levels which may be some 20 dB or more above the maximum input, the dynamic range of the system with the parameters described above is clearly inadequate. Further coherent integration in the beam-forming, pulse-compression and Doppler domains is difficult to achieve. A look-up table implementation, however, leads to a simple solution.

For a pulse chip-length of 10 μS, the front-end system bandwidth is 100 KHZ. Present-day memory chips have access time of <100 nS. A/D conversion is done by zero-crossing detectors and is, therefore, not a limiting factor to the sampling rate. Hence, it would be possible to sample and process the pulse at a rate of, say, 10 M-samples per sec, and use digital accumulators at the output of the first beam-forming stage to restore to the previous rate. In this way the noise bandwidth is opened up 100 times at the sampling point giving further margin for linearity. The original signal to noise performance is, of course, restored after the accumulation point.

Taking out 2 dB for digitisation loss and 9 dB to preserve linearity, the dynamic range of the example system is now:

$$66 + 20 - 2 - 9 = 75 \text{ dB}$$

Figure 4 shows a system schematic diagram incorporation the above features. The antenna array face 10 is made up of a large number of antenna elements (not shown). Each element feeds a zero i.f. channel 11, similar to that shown in Fig. 2, in which the A/D is effected by zero crossing detection to give 1-bit digital words I_s and Q_s. Sub-pulse sampling of the signals received at the antenna elements is performed at a high rate as previously described (sampling control not shown). A first beam-forming stage 12 is provided by a set of RAMs each of which is addressed by a group of digitised antenna signals which effectively form a multi-bit address for the RAM. The RAMs contain look-up tables in

which appropriate weightings are supplied by a beam controller 13. The outputs of the RAMs are unique multi-bit words. Successive outputs from each RAM are then fed to accumulators 14 in which the multi-bit words are integrated with respect to time as previously described. Additional stages of beam-forming, 15 and 16, may be incorporated to combine the output of secondary groups of multi-bit words from the accumulators 14 to provide both azimuth and elevation beam-forming, using similar look-up table procedures as adopted for the first stage, again with weightings supplied by the beam controller 13. The accumulation after the sub-pulse sampling is best done between the first and second beam-forming stages, to give a reasonable data rate for the latter. For an S-band radar, for example, the array size will be roughly of 4 m each side. Connecting signal and control wires between the various blocks is not a simple task. Signal coupling and driving/receiving problems must be carefully considered. One possible way is to mount the first and second stages of the beam-forming network directly onto the array face, and then bring the subsequent reduced number of signal lines to the third stage 16 down onto a main processing unit 17, where the pulse-compression, Doppler filtering and detection functions are also implemented.

Because of the large number of common components for the first stage of beam-forming, a common hybrid or monolithic pack may be the best solution.

CLAIMS

1. A digital beam-forming radar including an array of receiver antenna elements, means for simultaneously sampling the signals received at all the elements, individual digitising means for each element whereby successive signal samples received from each element are converted into respective one-bit digital words, a first beam-forming stage wherein first groups of simultaneously occurring digital words are presented in the form of multi-bit addresses to memories individual to each group, each memory holding predetermined look-up tables whereby each group address causes a first unique corresponding digital code word to be output from the memory, and means for applying the outputs of the first beam-forming stage to further beam forming stage(s).

2. A radar according to claim 1 including digital accumulation means for each memory in which a predetermined succession of code words from a memory are integrated with respect to time before being applied to the further beam forming stages.

3. A radar according to claim 1 or 2 including a second beam-forming stage wherein the outputs of the first beam forming stage are grouped together in secondary groups presented in the form of addresses to further memories individual to each secondary group, each further memory holding a predetermined look-up table whereby each secondary group address causes a second unique corresponding digital code word to be output from the memory, the secondary code words of the second beam forming stage being applied to a third beam forming stage.

4. A radar according to claim 3 including means for slicing the addresses for the further memories into groups of single bit significance, whereby each group is applied in turn to the memory addressing means, and means for recombining the subsequent outputs from all the look-up operations with appropriate weightings to arrive at a resultant output.

5. A radar according to any preceding claim wherein the sampling rate of the signals at the antenna elements is in excess of the minimum dictated by the sampling theorem and the outputs of the accumulation means are produced at not less than the minimum sampling rate dictated by the sampling thereon for sampling the signals at the antenna elements.

6. A radar according to any preceding claim wherein the look-up tables in the memories in the beam-forming stage(s) are provided with weighting functions from a beam control circuit.

7. A radar according to any preceding claim wherein the first beam-forming stage includes two sets of memories each having different look-up tables and switching means whereby the multi-bit addresses are presented to the two sets in succession.

8. A radar according to any preceding claim wherein the memories are random access memories (RAMs).

9. A radar according to any preceding claim wherein the first groups of digital words are each taken from a non-uniform arrangement of antenna elements.

10. A radar according to any preceding claim wherein the individual digitising means for each element comprises a zero i.f. channel wherein the incoming signal is split into two paths and mixed with two local oscillator inputs in quadrature at the i.f. frequency, the resultant baseband signals being amplified, filtered, sampled and held and then applied to analogue to digital converters (A/D) to produce in-phase and quadrature output words.

11. A radar according to claim 10 wherein the A/D converters are zero-crossing detectors.

12. A digital beam-forming radar substantially as described with reference to the accompanying drawings.

13. A method of digital beam-forming in a radar having an array of receiver antenna elements including the steps of simultaneously sampling the signals received at each of the elements, individually digitising the sampled signals into respective one-bit digital words, applying first groups of simultaneously occurring digital words to memories individual to each group whereby each group forms a multi-bit address for a memory, each memory holding predetermined look-up tables whereby each

address causes a unique corresponding digital code word to be output from the memory.

14. A method according to claim 13 including the steps of integrating a succession of code words from each memory with respect to time.

15. A method according to claim 13 or 14 including the steps of grouping together outputs of the memories in secondary groups and presenting the secondary groups of words as addresses to further memories individual to each secondary group, each further memory holding a predetermined look-up table whereby each secondary group address causes a second unique corresponding digital word to be output from the memory, and applying the secondary code words to a further beam-forming stage.

16. A method according to claim 13, 14 or 15 including the steps of slicing the addresses for the further memories into groups of single bit significance, applying each group in turn to the memory addressing means and recombining the subsequent outputs from all the look-up operations with appropriate weightings to arrive at a resultant output.

17. A method according to any one of claims 13—16 wherein the sampling of the signals at the antenna elements is effected at a rate in excess of the minimum dictated by the sampling therein and the number of successive code words integrated in the accumulator is such as to produce accumulator output words at the minimum sampling rate.

18. A method according to any one of claims 13—17 including the step of applying to the memory look-up tables weighting functions determined by the beam controller.

19. A method according to any one of claims 13—18 wherein the signals received at each antenna element are mixed in quadrature with a local oxcillator signal at the intermediate frequency, the resulting zero, i.f. signals being amplified, filtered, sampled and held and then being digitised.

20. A method according to any one of claims 13—19 wherein the digitising of the sampled signals is effected by determining zero crossing of the signals.

21. A method of digital beam-forming in a radar substantially as described with reference to the accompanying drawings.

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